



Development of Production PVD-AlN Buffer Layer System and Processes to Reduce Epitaxy Costs and Increase LED Efficiency

SSL MFG R&D Workshop, San Jose, CA

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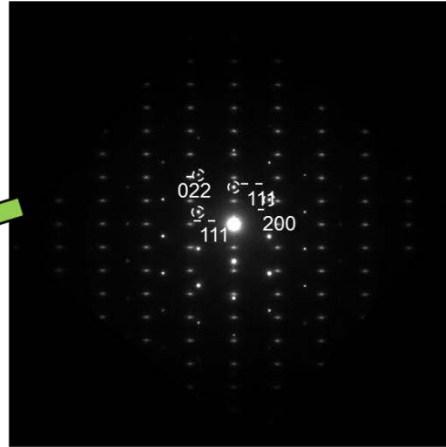
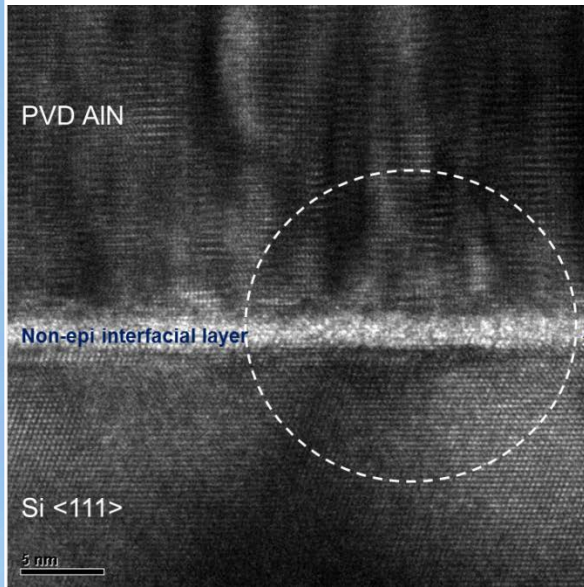
Project Objectives

- 60% reduction in epitaxy manufacturing costs
 - Cost of Ownership reduction using higher throughput PVD AlN buffer
 - Reduction in defect density with PVD buffer (higher brightness)
 - Reduction in non-ESD yield loss through reduction in wafer bow and temperature variations
 - Enablement of GaN/Si processing with PVD buffer
- Phase I – Process Development – GaN on Si
 - PVD AlN buffer for GaN on Si
 - Epitaxial growth
 - Protection of Substrate from subsequent GaN deposition (Ga chemistry)
 - Stress/Strain control
- Phase II - High Volume PVD AlN Buffer Tool
 - Design, build, qualification of system
 - Process transfer
- Phase III – Throughput Enhancement
 - In-situ cleaning capability
 - CoO Reduction demonstration

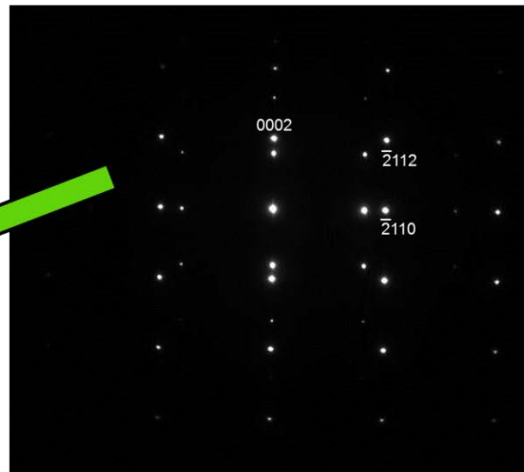
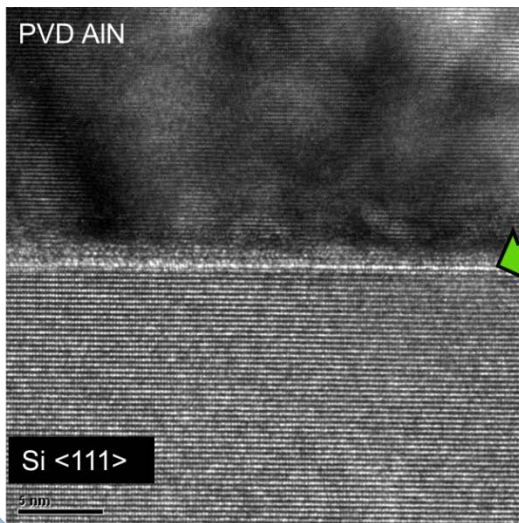
Year One

Year Two

Epitaxial Growth



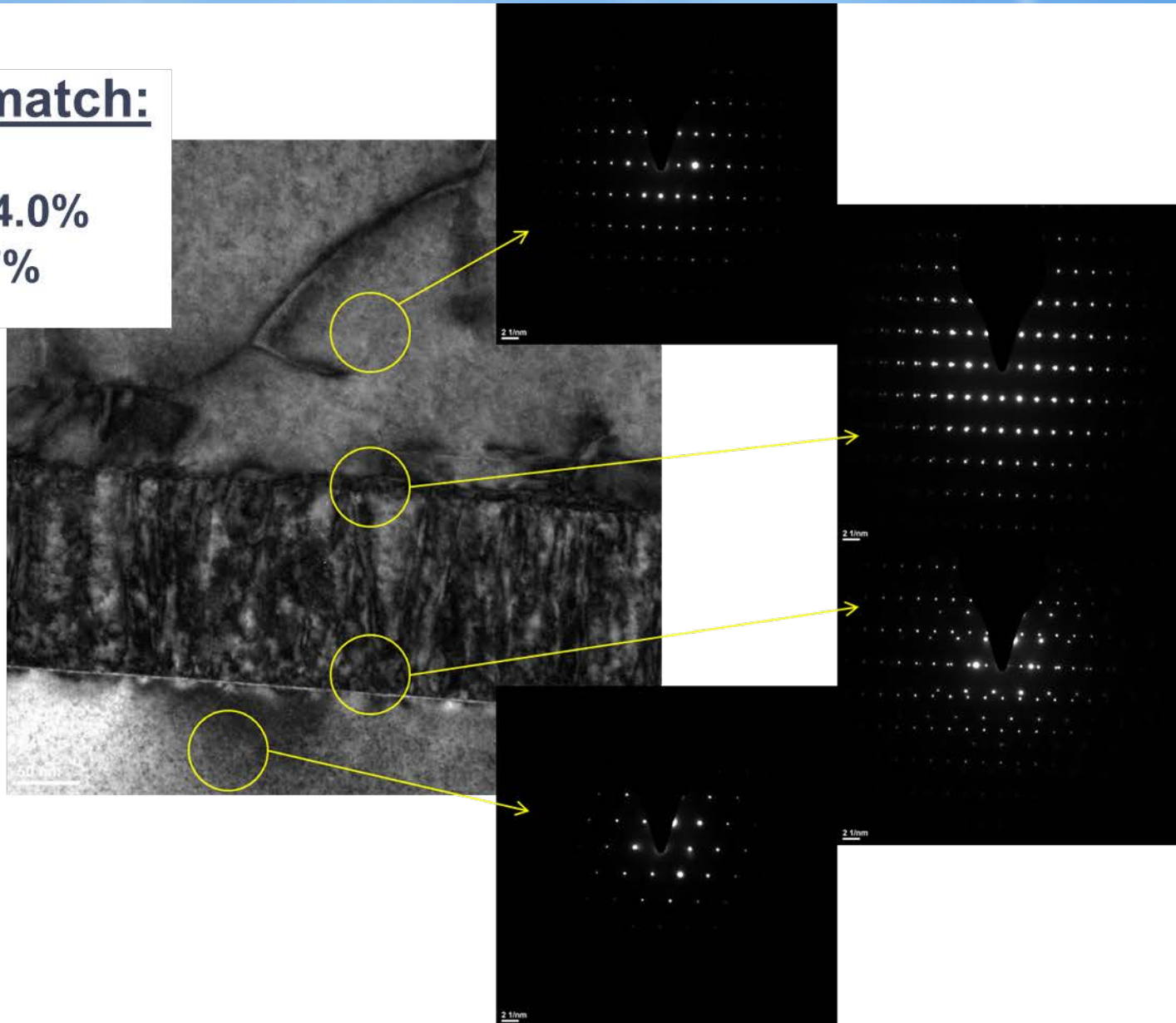
- Epitaxial quality buffer layers achieved with PVD deposition!!
- Further progress made to reduce non-epi interfacial layer and improve PVD AlN film quality



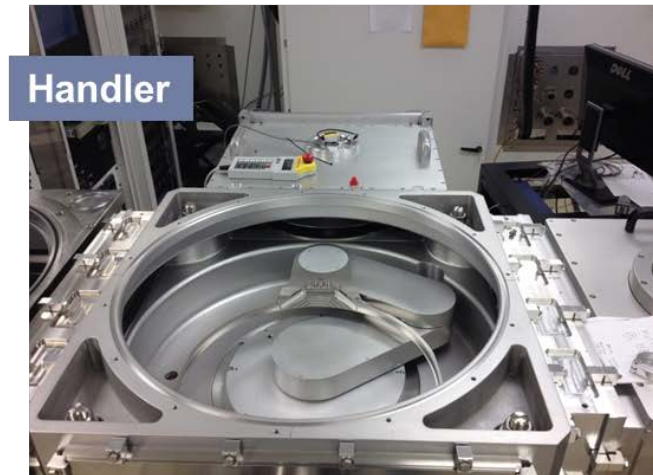
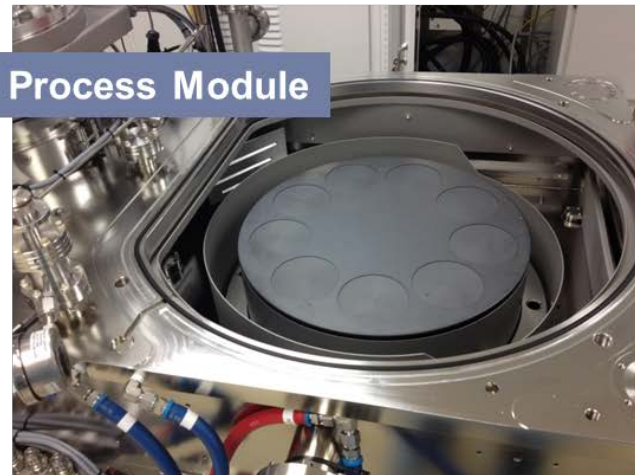
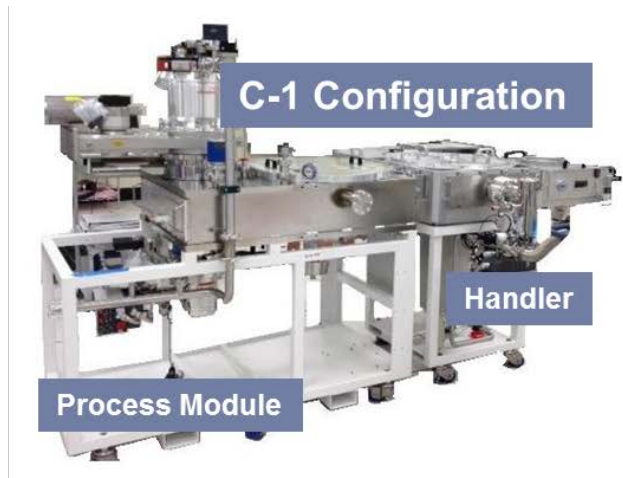
Epitaxial Growth

Lattice Mismatch:

- $\text{GaN}/\text{AlN} = 4.0\%$
- $\text{AlN}/\text{Si} = 5.7\%$



High Volume Manufacture PVD AlN Buffer Layer Tool System Currently Under Test



- High Volume Manufacturing System Development progressing to schedule

Conclusions

- All of the tasks for Phase I and II have been completed
- Two milestones to be met - achievable by September
 1. Further AlN film quality improvement
 2. Complete elimination of Si melt back to meet GaN targets
- Process qualification (demo readiness) by end of September